DESIGN OF SRAM IN SUBMICRON TECHNOLOGY USING VLSI

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Abstract - Designing a chip has low power becomes major challenge of present time. Design of SRAM implies power has been increasing with scaling of technologies. As modern technology is concerned, it is very important to design lower power, high performance and fast responding SRAM(Static Random Access Memory) therefore they are critical component in high performance processors. The conventional 8T SRAM cell is very much create noise during read operation. To overcome this problem, researchers have proposed different SRAM topologies such as 6T bit cell design. These 6T bit cell design can improve the cell stability but suffer from bitline leakage noise. In this paper, work at SRAM memory has been designed to overcome power consumption problem. and also improves the cell stability by increasing Read Static-Noise-Margin.

Keywords-CMOS logic, SRAM, VLSI, Read Static Noise Margin, stability and power consumption.

I. INTRODUCTION

The memories are classified in the ways that information is stored which are two types, Non-volatile memory and Volatile memory. When the data is stored Non-volatile memory, even when the power supply is turn off, the data remains stored. And when the data is stored in volatile memory then power supply is turn off then the data is lost. There are two types of volatile memory, Static and Dynamic .these can be classified by their clock frequency. The Static memories have no requirement on the slowest clock rate. Whereas dynamic requires periodic clock to refresh stored information .this memories may be used as in embedded form in all kinds of controller and microprocessor. SRAM or Static random Access memory is a simple form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated as in the case of DRAM memory. There are two key features to SRAM (Static random Access Memory), and these set it out against other types of memory that are available:

1. The data is held statically: This means that the data is held in the semiconductor memory without the need to be refreshed as long as the power is applied to the memory.

2. SRAM is a form of random access memory: A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed.

Static memory is a high speed memory. Static RAM is a type of RAM that keeps the data that is fed to it, without it having to be rewritten over and over. Dynamic RAM is also one type of the RAM, the first difference is that for DRAMs, to keep the data that is stored from being lost, has to be refreshed by writng the same data to it over and over again with circuitary like pen that dispenses disappearing ink into paper. The second difference is that SRAMs are used for specific application within the PC.where their strength outweighs their weaknesses compared to DRAM. For SRAM,each bit is composed of between four and six transistors, the part that hold information , which is why SRAM takes up much more space compare to DRAM.to compare with SRAM , DRAM has only one transistor plus capacitor acting like miniature rechargeable battery. For high performance VLSI circuit in system-on-chip,SRAM is used due to need of battery.

The individual SRAM memory cell circuit which consists of four transistors configured in which two are cross-coupled inverters. The circuits having two are stable states.and these equate to the logical ‘0’and ‘1’states. In this format, additional two transistors are required to control access to the memory cell while read and write operation. This makes total of six transistors, making termed 6T memory cell. Any three terminal switch device can be used in SRAM, MOSFETs and In CMOS technology is used to ensure that very low levels of power consumption are achieved. Extending with semiconductor memories to very large dimension, each cell must achieve very low level of power consumption to ensure that the overall chip does not dissipate too much power.

II. TYPICAL SRAM ARCHITECTURE

The operation of the SRAM memory cell is straightforward. If the cell is selected, the any value to be written is stored, the any value to be written is stored in the cross-coupled filp-flops.All the cells are arranged in the matrix formed. With each cell individually addressable. Most SRAM memories select entire row of cells at a time. And the content of all the cells in the row read out along the column lines. Even if it is not necessary to having two bit lines, by using the signal and its inverse, this is normal practice which improves the noise margin and improves the data integrity. the two bit lines are passed through to two input port on comparator to enable the advantages of the differential data mode to be accessed and small amount of voltages swings that are present can be more accurately detected.

A cell design to eliminate the limitation is sis replaced by PMOS transistor. This SRAM cell is consists of six transistors, out of them one is NMOS transistor and one is PMOS transistor for each inverters. Add two NMOS transistors connected to the row line. This configuration is called as 6T cell. This cell gives better electrical performances (speed, noise immunity etc.). This 6T cell architecture was reserved for niche markets such as military or space that needed high immunity components.

2.1 System Development

The Classification of memory circuits are depend on the data storage and the type of the data access ROM is a volatile that means Permanent memory. If we write a data storage function and then the power supply is off then we can't lost a data.

The read/write memory gives permission for modification of data bits. But the read/write memory need the data storage function be volatile. This memory is also called as RAM (Random Access Memory).

Fig 2.1 shows the typical memory array organization. It consists the individual memory cell which is arranged in horizontal rows and vertical column. Each cell of memory stored a one bit of binary information. The total number of memory cells in this array is 2*2.

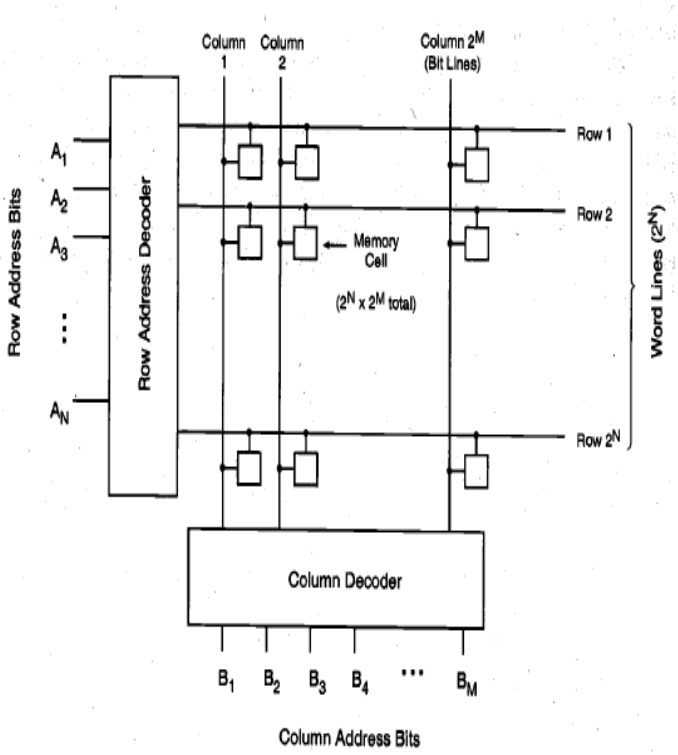

Figure.2.1. Typical Random Access memory Array Organization

For the perfect data bit in the array we need to activate the bit line and word line. The row and column selection procedure carry out by the decoder of row and column respectively. Here the array organization also called as a Random Access Memory. And used for the both the operation read-write memory arrays and read only memory arrays.

For the implementation of memory cells we used a two technologies i.e. RAM (Static Random Access Memories) and DRAM (Dynamic Random Access Memories). We used six transistors for the designing of SRAM cells. The purpose of using 6T cells it is designing for speed.

2.2 SRAM Cell

The need of a designing SRAM is to providing a direct interface with the other device and replaces such type of devices which require low power consumption for e.g. DRAM.A PC microprocessor memory configuration which include the internal cache memory, external cache memory and the main memory. For the modification of data bits we need a permission that's why we design a read/write(R/W) memory circuits. The memory circuit operates without refresh operation. The RAM cell contains two cross coupled inverter and two transistors. The devices used in SRAM are made up of polysilicon resistors, N-MOS transistors/ P-MOS transistors, and

type of memory cell. There are many layers are available and these layer are made up of polysilicon, one layer is used for the enhancement-type N-MOS transistor and another layer is used for load resistors and interconnects. For the reducing the current flow through the memory cell. We used high valued load resistor. For the use of memory cell we get static characteristics and better noise margin than the resistor load cell.

2.3 SRAM Memory Architecture

The Architecture of SRAM memory which is asynchronous design having memory locations in random order at a fixed rate. The storage array made up of cells circuits which is shared a connection in horizontal rows and vertical column. The horizontal lines which is outside the storage array which is called as word line and vertical line along which data flow into and out of cells are called as a bit lines. A cell is used for reading and writing by selecting row and column and the cell can store 0 and 1 bit.

The Architecture of SRAM includes one or more rectangular arrays of memory cell which is support to the decode addresses and implement the required read and write operation. The another circuitry which is used for the implement of special features i.e. burst operation.

III.MEMORY COMPONENT FOR SRAM

3.1 Decoder

Decoder is a combination of more than two AND gates using true and complementary versions of address bits. The Architecture of SRAM consists of SRAM decoder circuit, decoder driver circuit, WR logic circuit sense amplifier. The size of a decoder matched to memory array that means height of a decoder gate must match height of a row. The height of a decoder is large with the number of inputs that means if the input is increasing the height of a decoder is increasing. The AND gates programmed by connecting a polysilicon inputs to the address inputs. Decoder has a address decoder and row decoder.

3.2 SRAM cell read/write operation

The read/write operation of an SRAM is as shown in fig.to select a cell, the two access transistors must be 'ON' therefore the cell (flip-flop) can be connected to the internal SRAM circuit. This two transistor of cell are connected to the wordline.the selected word line will be set at Vcc. The flip-flop sides are connected to a pair of lines, B and B bar. The bit lines are known as columns.

During read operation, the two bit lines are attached to the sense amplifier that recognizes if logic data '1'or '0' is stored in the selected elementary cell. This amplifier transfers the logic state to the output buffer which is connected to the output pad. Read cycle starts with pre-charging BL and BL bar to 1 i.eVDD.Within cell M1 and M4 are turn-on. Asserting word line, turns ON M5 And M4 are turn-ON. Asserting word line, turn ON M5 and M6 and the values of Q and Q bar are transferred to bit lines (BL and BLB). There is no current flows through M6 and M4 and M6 pull BL up to VDD, i.e. BL=1.BLB discharges through M1 and M5. This voltages difference is sensed and amplified to logic levels by sense amplifiers.

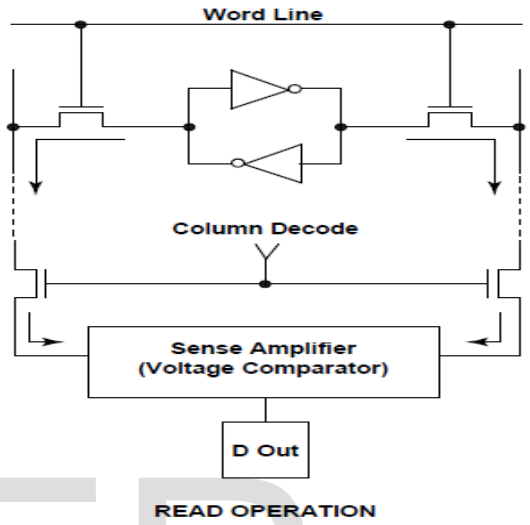

Figure.3.2 (a): SRAM Cell Read Operation

During write operation, the data comes from the input pad. Then it moves to write circuit. Therefore the write circuit drivers are strong as compare to the cell flip-flop transistor. The data will be forced onto cell. When the read/write operation is completed, then the word line is set to 0 V and the cell (flip-flop) either carry its original data for read cycle or stores a new data which was loaded during the write cycle. The value to be written is applied to the bit lines. Therefore to write data '0',we assert BL=0, BLB='1' and to write data '1','the BL='1' , BLB='0'.asserted when WL=1.

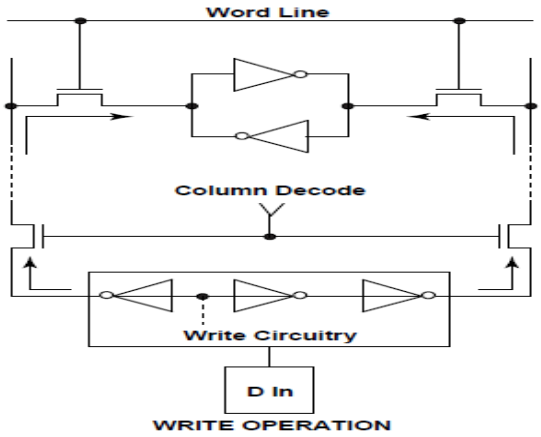

Figure 3.2(b): SRAM Cell Write Operation

3.3 Memory cell

An SRAM memory cell is bistable flip flop making of 4 to six transistor. The flip-flop may be two states that can be interpreted by the circuit to be 1 or 0. Most of the SRAMs on the market use a four transistor cell with polysilicon load. Suitable for medium to high performance, this design has relatively high leakage current and consequently high standby current. Four transistor design may also be various types of radiation induced soft errors. IBMs SRAM all use 6 transistor memory cell that is highly stable, relatively impervious to soft errors and has low leakage and standby currents. The sizes of the cell array depend on both performance and density requirement. Generally as technology shrinks, cell array are moving from tall to write structures. However, since wider arrays need more circuitry for column multiplexers and sense amplifier if a small area overhead is desirable, the no of rows is kept high the data storage structure consists of individual memory cell arranged in array of horizontal rows and vertical column. Each cell is capable of storing one bit of binary information. The size of the cell array depends on both performances and density requirements. Generally in this structure, there are 2N rows, also called word line and 2M columns also called bit line thus the total no. of memory cell in this array is 2Nx2M.

3.4. Software Description

The present experiment is a guide to using the <<Microwind>>educational software on a PC computer. The Micro wind program allows the student to design and simulate an integrated circuit. The package itself contains a library of common logic and analog ICs to view and simulate Micro wind includes all the commands for a mask editor as well as new original tools never gathered before in a single module. You can gain access to circuit simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.A specific command displays the characteristics of pMOS and nMOS, where the size of the device and the process parameters can be very easily changed. Altering the MOS model parameters and, then, seeing the effects on the Vds and Ids curves constitutes a good interactive tutorial on devices. The process simulator shows the layout in a vertical perspective, as when fabrication has been completed. This feature is a significant aid to supplement the description of fabrication found in most textbooks

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IV. CIRCUIT DESCRIPTION

The 6T SRAM circuit consists of six transistors. And the four transistors are in the Centre form two cross-coupled inverters. If we give a low input to the first inverter it will generate high value on the second inverter which amplifies and store the low value on the second inverter. Similarly ,a high input value given to the first inverter it generate low input values on the second inverter which feedback the low input value onto the first inveter.these two inverters will store their current logical value. Whatever value that is low or high.

The lines of inverters are connected to two separate bitlines.the gates of these transistor are driven by word line. The word line is used for in target SRAM.the SRAM stores its current value.

When the word line is high ,both N-channel transistor are conducting and connect the inverter input and output to the two vertical bit lines. The data can be amplified and generates the output value of the SRAM cell in read operation. T0 write a data into the memory the word line is activated and the bit line are also activated. Depending on the current value stored inside the SRAM cell there might be a short-circuit condition, and the value inside the SRAM cell is overwritten. This only works because the transistors inside the SRAM cell are very weak.

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have “readability” and “write stability” respectively.

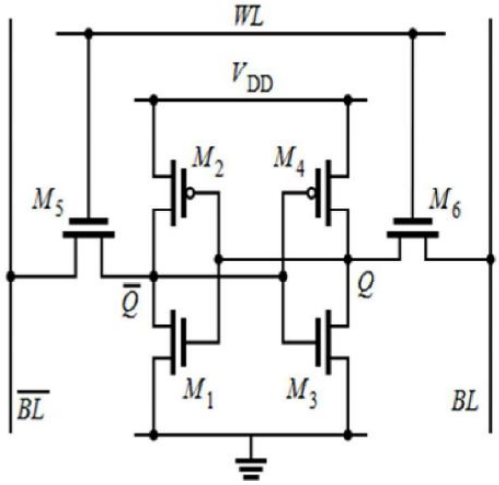


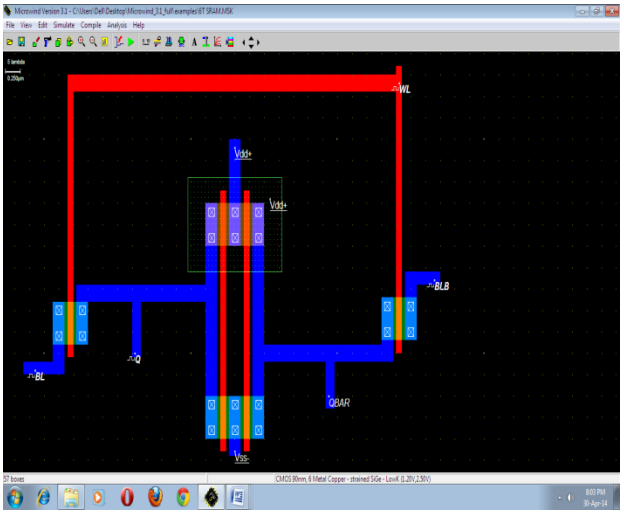
Figure.4.1:.A 6T SRAM Circuit

V.RESULT ANALYSIS

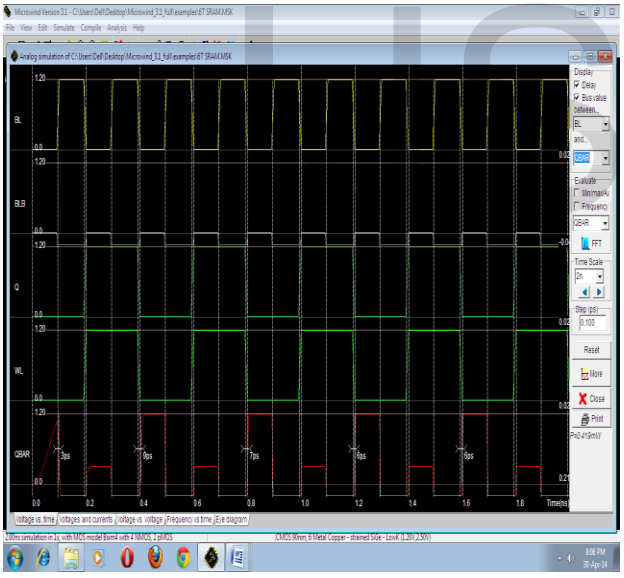
To design a device which is more than one port, which may be useful in register files implemented with multi-ported SRAM circuitry. The six transistor SRAM provides in density at the cost of

manufacturing complexity. We got a result of 6T SRAM consumes low power for the operation and it take small area. Also reduce extra time for the complete operation. The static RAM used in various categories of industrial and scientific subsystem.

Layout of 6T S RAM



Result:



VI. CONCLUSION

Design the new load less 6T SRAM. 6T SRAM array consumes Low power with low area. Also reduce access time and stability. The sum of power consumption in decoders, bit lines, and periphery circuits represent the active power consumption. Nanoscale CMOS SRAM memory because it reducing noise margin and increasing variability, due to the continuous technology scaling. Previous transistors i.e. 10T, 9T, 8T are required more power consumption as compared to 6T SRAM.

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